SOFTWARE DEFINED RADIO ARCHITECTURES
FOR
MOBILE COMMERCIAL APPLICATIONS

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ABSTRACT

The commercial application of Software Defined Radio (SDR) has been a complex endeavor. Even as SDR solutions for wireless applications have emerged in the market, the power and performance requirements of mobile devices continued outpace SDR's development. While SDR solutions appeared to address the growth in allocated spectrum and protocols with a flexible solution, those existing SDR solutions were unable to support the small form factor and low cost requirements of the portable device industry.

Designers of multimode devices have had limited choices in multi-band/multi-protocol radio architectures. Designers could either switch between a set of single function transceivers implemented on a single die or in a single package, or designers could implement what's been considered the traditional SDR approach, a high bit rate – high sampling frequency analog to digital converter (ADC) immediately following the antenna with sophisticated high performance DSP processing. Design choices were limited. Designers could choose either a fixed purpose multimode radio with limited flexibility and lower power consumption or a more flexible SDR solution with higher power consumption. The higher power required when using a wide band ADC is one of the primary reasons why SDR solutions have been successful in infrastructure but not mobile solutions. Infrastructure SDR equipment with less demanding power constraints has already been shipping commercially for some time.

The Softransceiver™ RFIC architecture addresses the growing need for reconfigurable multimode battery operated devices in the commercial marketplace. This architecture successfully blends the performance of analog transceivers with the flexibility of digital programmable circuits. BitWave Semiconductor redesigned transceiver functional blocks to enable dynamically reconfigurable circuits, implemented CMOS fab processes which support low cost and high yield silicon production and chose a largely digital architecture to allow for a highly scalable implementation. Software Defined Reconfigurability is thus achieved while also hitting commercial wireless benchmarks for power, performance and cost.

1. INTRODUCTION

There are many frequency bands and protocols for entertainment, data and communications. In spite of the best efforts of regulatory bodies to promote national and international standardization, competition driven by the continuously growing demand for wireless services has stimulated the commercial world to create a diverse set of networks. While each separate regulatory body specifies the array of frequency bands and protocols for the services they'll permit to be deployed in a geographic area, it's the service providers who select the actual frequency band and protocol over which they deploy their services. That is not to imply that each business creates strategy and policy in a vacuum. There is a clear business benefit to global standards. Most standardization efforts strongly advocate wide adoption of their standard. In spite of this, there are still discontinuities in coverage for many of today's desired wireless services. As a result, when new portable device vendors attempt to analyze the combinations of networks and protocols to determine the most profitable combination, it's often hard for the marketers and engineers to decide where to begin.

Deploying multifunctional audio, video and data devices across heterogeneous communication and entertainment networks understandably leads to complex device designs. In creating these multi-application services, wireless device designers have continued to integrate more and more functionality into handsets and other portable devices. These new services and the portable devices which support them continue to enhance the value of wireless communications in our society.

2. RECONFIGURABLE RADIO OFFERS SIGNIFICANT BUSINESS VALUE

The key to wide adoption of technologies such as reconfigurable radio is to ensure that the technology solution aligns closely with business requirements. Software reconfigurable radios offer clear advantages to wireless users and designers alike, however these advantages are not enough to drive widespread adoption unless the service provider can also realize compelling value from the technology. This requirement for "business value" means that the cost, power and performance of an SDR based solution must lead to improved customer satisfaction and improved business profitability. Until now, only markets that required reconfigurable radios and that were less price-sensitive could support SDR businesses. For example, many non-commercial applications required flexible multi-protocol frequency hopping radios. The primary benchmark for those devices was performance and flexibility. Cost, while always a concern, was less critical. Commercial markets have always demanded more attention to cost. Evolving SDR solutions so that they become attractive to broader wireless device markets can only happen with detailed and focused attention on price and power.

Consumers benefit from more device and application choice. With SDR enabled portable devices, consumers could buy a phone first and subsequently activate it on the network of choice or could benefit through post sale service activation.

MVNOs benefit from extraordinarily flexible device architecture. MVNOs could partner with multiple networks to deliver the same service or deliver one service over multiple networks. Either way, MVNOs have the freedom to partner with network resources for maximum business value unrestricted by the constraints of any particular protocol or frequency.

Carriers benefit from new opportunities to grow their network footprint and leverage the ensuing economies of scale through acquisition of heterogeneous spectrum and technologies.

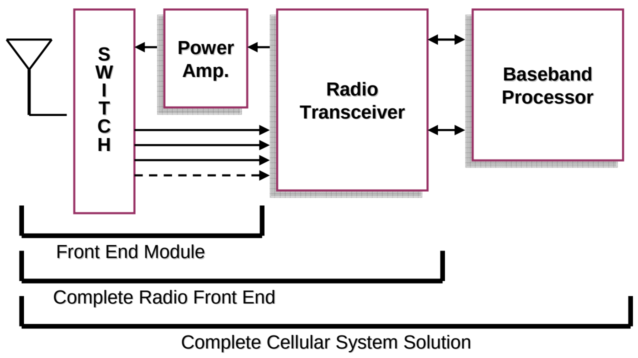
Device OEMs can realize supply chain improvements with substantial inventory reductions due to the development of standardized radio modules and platforms. Standardized reconfigurable radio platforms will directly translate into reduced time to market. Additionally reconfigurable radio solutions allow device OEMs to future proof their device capabilities.

New architectures such as that being developed by Bitwave have the potential to overcome the constraints of existing designs and architectures. Commercial application of these new architectures will depend on the "business value" they provide. Once deployed into a network and as the carrier requirements for multi-mode devices become more demanding, the value that these new architectures offer throughout the value chain will steadily increase.

3. LIMITATIONS OF TODAYS ARCHITECTURES

Today's wireless radio solutions can be modeled as three essential blocks, a front end module or FEM, a transceiver and a baseband modem (Figure 1).

Mobile Phone Architecture Schematic



Source: Citigroup Investment Research

Figure 1 – Architecture Schematic

The multi-function baseband modem, which typically consists of all digital logic, has successfully scaled with advancing process technology. As the leading edge process node has moved lower, the gate count in a modem has scaled geometrically higher enabling a rapid increase in the functionality delivered by the baseband. The increased computing power available in the baseband has contributed significantly to the creation of multimode baseband modems.

There has also been an ongoing effort to scale analog RF functionality with the process node. Analog designers also face multiple issues. Parasitic capacitance and inductance become more difficult to model as the process geometry advances. Leakage currents increase as gate widths become narrower. Passive components do not easily scale with process geometry.

Silicon transceiver designers have had a difficult time overcoming these limitations and have focused their effort to achieve their multi-mode wireless device cost and performance targets through integration. Multi-chip modules, multi-die in a package, multiple transceivers on a chip all serve to minimize cost. Yet integration of a switched set of single protocol transceiver does not address the underlying design problems associated with scaling RF devices.

Requirements	GSM	UMTS (FDD)	CDMA2000	WiFi (802.11g)	WiMAX (802.16d)
Maximum Instantaneous Dynamic Range	107	87	97	73	77
Channel Bandwidth	200 kHz	5 MHz	1.25 Mhz	20 MHz	Variable

Table 1 - Selected Performance Benchmarks by Protocol

4. ARCHITECTURAL INNOVATION

In Table 1, the range of performance required by the major wireless protocols in use today differs dramatically. A voice protocol such as GSM requires very high dynamic range due to its blocker profile but low bandwidth. More spectrum efficient protocols such as CDMA and UMTS require less dynamic range but more bandwidth. Short range broadband data delivered using WiFi requires relatively low dynamic range but high bandwidth. Because of the different applications for the many wireless protocols in use today and in the foreseeable future, no current single radio design could ever efficiently support the wide range of applications desired by consumers. The question for portable device designers and for the device OEMs is how to select an architecture and then design a radio that offers the most business value for their customers and implicitly that means the device designers must continuously attempt to optimize the cost and performance trade-off.

The key to creating a reprogrammable architecture for mobile devices is in blending high performance analog circuits with flexible and reprogrammable digital logic. BitWave's Softransceiver architecture combines analog and digital circuitry to produce a power-efficient yet flexible architecture which can be scaled to the chosen process node.

One key insight is in recognizing the need to design for a performance envelope (Figure 2). Past architectures have often been designed to cover all the corner cases simultaneously. However, in recognizing that different protocols require different performance envelopes, BitWave made an intuitive leap and inferred that a flexible architecture could enable a smaller circuit which could be reconfigured to meet the individual performance specification illustrated below.

BitWave's systems engineering team played a key role in identifying which performance criteria could be traded off within the silicon circuits that were designed. Many system level parameters such as linearity, noise figure, power, IP3, and dynamic range are interdependent. This provides the designer with a large number of alternatives. For example in the Softransceiver architecture, for a given Signal to Noise Ratio (SNR), Sample Rate (F_s) and analog baseband filter order can be successfully traded off against one another. Bit Energy or Enob (which correlates to F_s) can be increased either by high oversampling or through a higher number of quantized bits.

This flexibility changes many design paradigms currently being followed. Where the current traditional SDR architecture would require a designer to find a high sampling rate yet low power ADC which could cover the extreme performance corners, the Softransceiver™ architecture enables implementation of a flexible ADC which can be reconfigured to deliver only the specific performance required by the selected protocol. The reconfigurable architecture along with careful design choices enables the creation of an area efficient circuit with high gate utilization in each of the selected modes.

Further demands are placed upon radios in that portable device designers must ensure that the radio is capable of robust performance in many diverse operating environments. The different protocols have different blocker profiles. Those profiles drive many different requirements on system linearity. Table 2 illustrates one

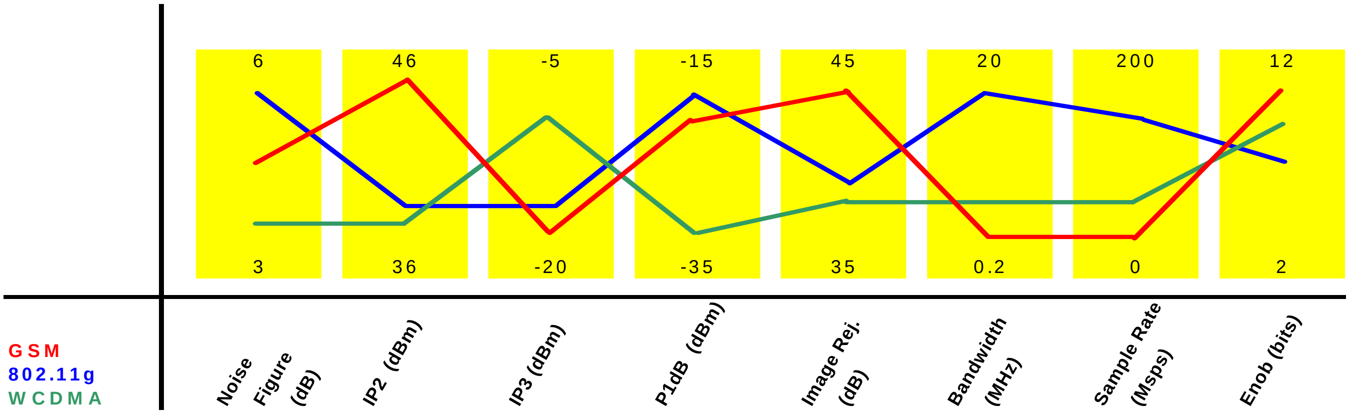


Figure 2 – Performance Envelope

	GSM	UMTS (FDD)	CDMA2000	WiFi (802.11g)	WiMAX (802.16d)
Noise Figure (dB)	3.4	3.2	5	5.6	Various
IIP3 (dBm)	-18.6	-17.6	-13.5	-20	-20
ADC Dynamic Range (dB)	57	47	62	53	55.4
Phase Noise	-146 @ 3 MHz	-150 @ 20 MHz	-146 @ 1 MHz	< 1.0° RMS	< 1.1° RMS

Table 2 - Softransceiver Minimum Expected Performance

possible set of minimum expected performance requirements for the Softransceiver. These performance targets are achieved through the performance tradeoffs discussed earlier.

Intuitively most engineers *know* that there is no free lunch. They *know* you can't build an extremely flexible architecture without paying a penalty in some key metric. BitWave is not violating any fundamental laws of physics. Rather, BitWave has identified a path to optimize the performance and size of the transceiver block level components ensuring there is no underutilized die area. By modeling the Softransceiver to demonstrate how gain, linearity and noise figure can be redistributed across the entire transceiver, the Softransceiver™ RFIC can meet the varying performance requirements of the different wireless protocols with minimal die area and power.

The Architecture

The first priority was to understand the tradeoffs between design performance and business value. Under guidance from systems engineering, BitWave's ASIC designers partitioned functional blocks using a mix of analog and digital design tools. This effort led BitWave to several innovations.

At the system level, BitWave created firmware which could monitor, manage and optimize individual block performance. As with traditional SDR architectures, the operating system is one of the essential pieces in implementing the programmable architecture. BitWave's object oriented application programming interface (OOAPI) enables virtual control of the various transceiver elements and their associated system level performance benchmarks. BitWave's configuration and control strategy enables system driven block configuration to deliver unprecedented low power and low cost radio solutions. BitWave's OOAPI control the radio core directly in realtime. This results in quick and dynamic block configuration whose performance envelope is easily shifted within a few clock cycles.

Proprietary low overhead algorithms manage this dynamic set up and calibration. The Softransceiver™ RFIC reconfigures itself in slightly less than the synthesizer settling time.

At the block level, BitWave created smaller, high performance programmable analog blocks. A smaller high performance implementation of a traditional analog architecture was developed based on the BitWave engineering team's aggregate experience and proprietary IP. This high performance radio core was built using a digital CMOS fab process and is one of the *smallest, scalable* radio cores in the world.

Softransceiver performance expectations have been measured through BitWave's IP validation and product demonstration tapeouts. As is shown below in Figures 3 and 4, BitWave's blend of analog and digital design has enabled a low k_{vco} and correspondingly low phase noise in the voltage controlled oscillator (VCO). Measured phase noise at the 3 MHz offset is below -141 dBc/Hz. This phase noise performance is achieved with a VCO core area < 0.2 mm^2 and which consumes < 3mW. Since completing this 2005 tapeout, BitWave has continued to improve overall chip performance. Current implementation meet the appropriate specifications.

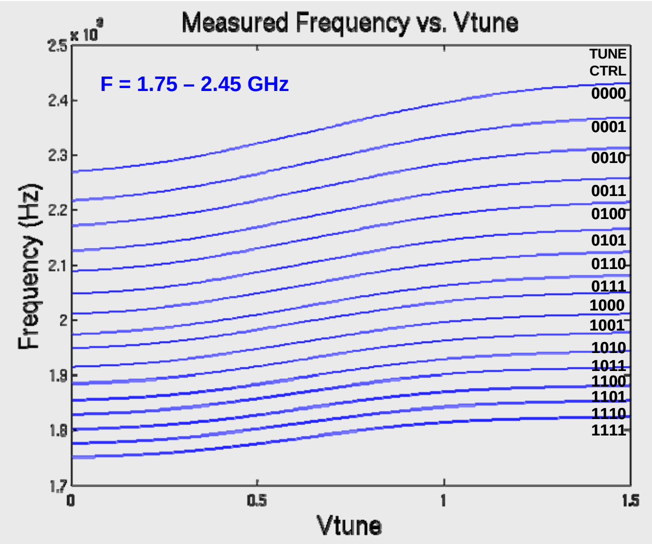
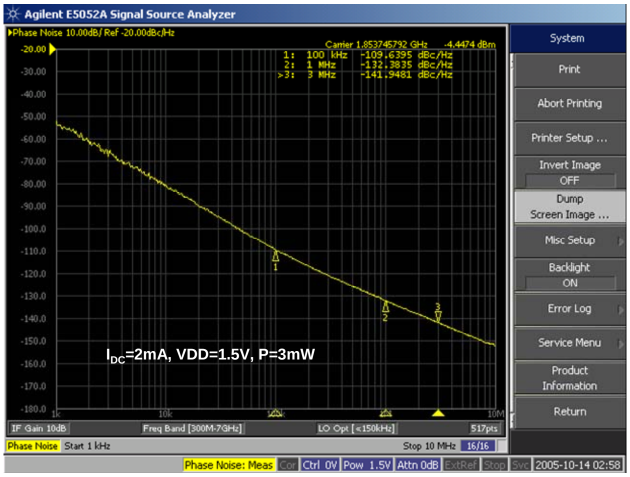


Figure 3 – VCO Vtune vs. Frequency

BitWave has also successfully demonstrated a narrowband low noise amplifier (LNA) tunable over a wide frequency range. LNA performance is shown in Figure 5. The same LNA is capable of producing dramatically different gain after programming the corresponding 4 bit control word via BitWave's OOAPI. In Figure 5, the shift in frequency along with the change in gain bandwidth is clearly evident. This LNA was completed in 0.15 mm^2 of die area and consumes only 6 – 9 mW of power.



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Carrier 1.853745792 GHz    -4.4474 dBm
 1:  100 kHz    -109.6395 dBc/Hz
 2:  1 MHz      -132.3835 dBc/Hz
>3:  3 MHz      -141.9481 dBc/Hz
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I_{DC}=2mA, VDD=1.5V, P=3mW

Figure 4 – VCO Phase Noise Performance

BitWave's BW1102 Softransceiver™ RFIC (Appendix 1) has been designed for mobile markets in general and optimized for cellular handsets. The BW1102 is designed for leading edge performance (linearity, noise figure, power) yet is price competive with single function single application transceivers. The Softransceiver™ RFIC is designed to meet the needs of todays and tomorrows handset designs. Particular care and effort has been taken in balancing cost and peformance.

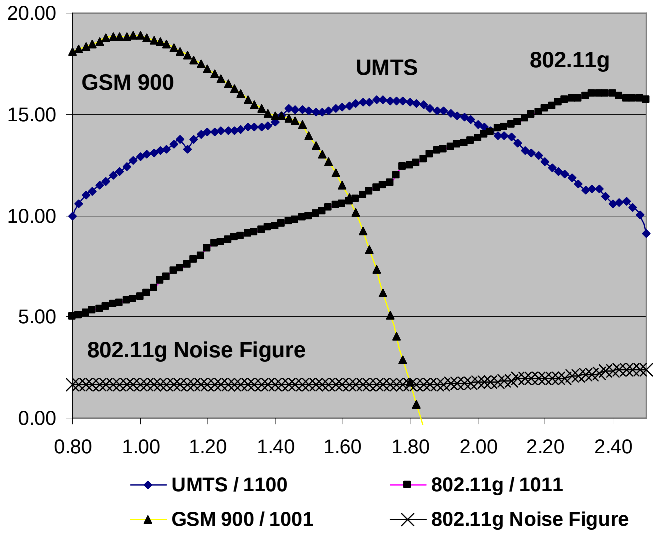

Figure 5 – Measured LNA Gain vs Frequency

SUMMARY

Many SDR implementations have succeeded in delivering the performance necessary to support multi-mode radios in selected cost insensitive markets. However those same implementations have been unable to deliver the business value necessary for mass market deployment in battery operated devices. Reconfigurable radio appears on the roadmap of most device OEMs, but before we see a network wide deployment of flexible devices, component suppliers must ensure that their next-generation radios deliver the needed business value.

New architectures found in transceivers such as BitWave's Softransceiver™ RFIC have the potential to overcome the problems of the past. Software reconfigurable radios offer clear advantages throughout the wireless value chain. Consumers, MVNOs, Carriers and Device OEMs will all benefit from the power of programmable radio to create new choices in device design and network architecture.

Software defined radio offers unique capabilities for the design and implementation of wireless devices and infrastructure. The key to widespread adoption is to ensure that the technology solution aligns closely with business requirements. BitWave's low cost, power efficient Softransceiver™ RFIC is anchored by efficient integration of analog and digital technologies. There is little doubt that the low cost, low power flexibility found in architectures like the Softransceiver™ RFIC's will be a necessary component in next generation wireless devices.

APPENDIX

The Softransceiver™ RFIC (BW1102)

One continously tunable transmit channel
One continuously tunable receive channel

RF Tuning Range

- **700 MHz – 4200 MHz**

Protocol Bandwidths Supported

- **Up to 20 MHz**

Standards Supported

- **UMTS (GSM, GPRS, EDGE, W-CDMA, HSDPA)**
- **CDMA2K (IS-95B, 1xRTT, EV-DO)**

- **802.11b/g, WiMax, WiBro**
- **iDen, AMPS, PHS, IS-136**
- **DVB-h, DVB-T, DTV, ISDB-T, DAB**
- **BlueTooth, GPS**

<u>Modem Interface</u>

- **3G DigRF plus extensions**
- **BWS Interface**

<u>FEM Interfaces</u>

- **Multi-port, Single-band**
- **Single-port, Multi-band**