

**Implementation of a Dual-Mode SDR Smart Antenna  
Base Station Supporting WiBro and TDD HSDPA**

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and decoding). Fig. 2 shows the WiBro transmitter and receiver block diagram.

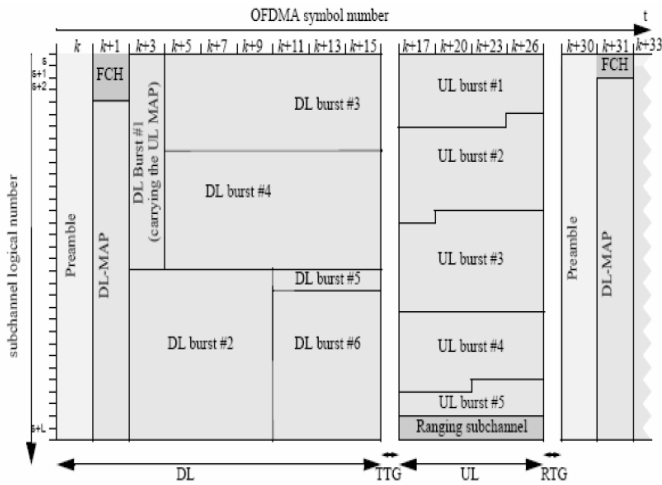


Fig. 1: WiBro frame structure

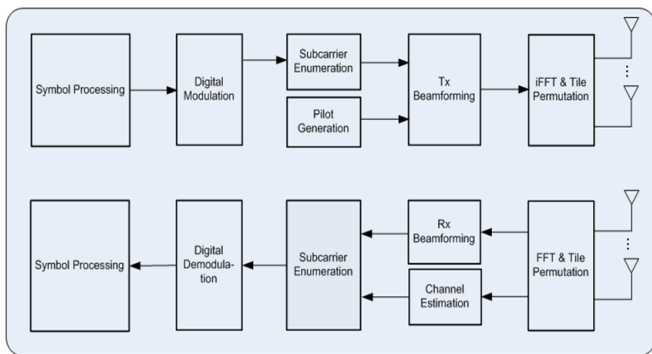


Fig. 2: WiBro block diagram

## 2.2. TDD HSDPA

The demand for high-speed packet data service increases rapidly. TDD HSDPA enables higher data rates in wireless communication. Specifically, this technology provides efficient downlink transmission at higher speed for multimedia service. TDD HSDPA can share the frequency bandwidth with the existing narrowband WCDMA system using 1.28 Mcps chip rate.

The TDD HSDPA frame for narrowband WCDMA has 10 ms duration, divided into two 5 ms subframes. Each subframe consists of 7 time slots. Between the first downlink and the second uplink time slots a downlink pilot, guard period, and uplink pilot are inserted. Each time slot has two 352-chip data fields, a 144-chip midamble for channel estimation, followed by guard period as shown in Fig. 3.

The TDD HSDPA uplink received signals are decomposed into several physical channels using OVFS,

demodulated and detected using estimated channel information obtained at midamble duration, then passed through symbol processing block as shown in Fig. 4.

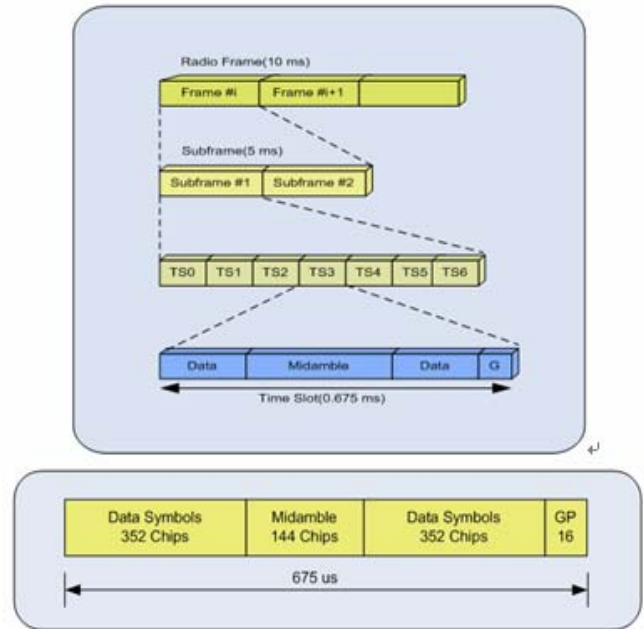


Fig. 3: Frame and time slot structure of TDD HSDPA

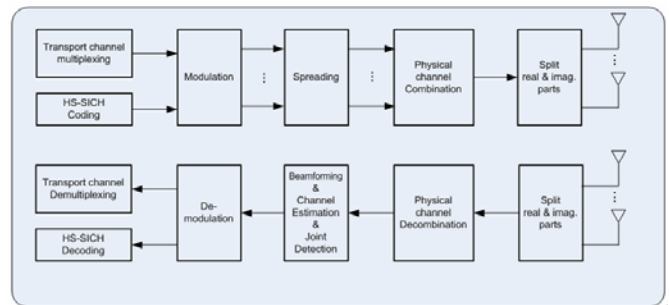


Fig. 4: Block diagram of TDD HSDPA

## 3. IMPLEMENTATION OF SMART ANTENNA CHANNEL CARD

### 3.1. Architecture of Channel Card

The proposed smart antenna channel card, described by Fig. 5 and Fig. 6, is implemented using several programmable devices for baseband signal processing: 8 DSPs, 2 FPGAs, and a microprocessor, as well as general-purpose interfaces such as LVDS and Ethernet for data exchange with external cards. To support the multimode and SDR concepts, the programmable devices are inter-connected with general interfaces and symmetric topology. Furthermore, device clock signals are available either from an external clock source or controlled by internal clock source and FPGA.

The proposed channel card is thus a flexible hardware platform, reconfigurable through software download for multiple modes.

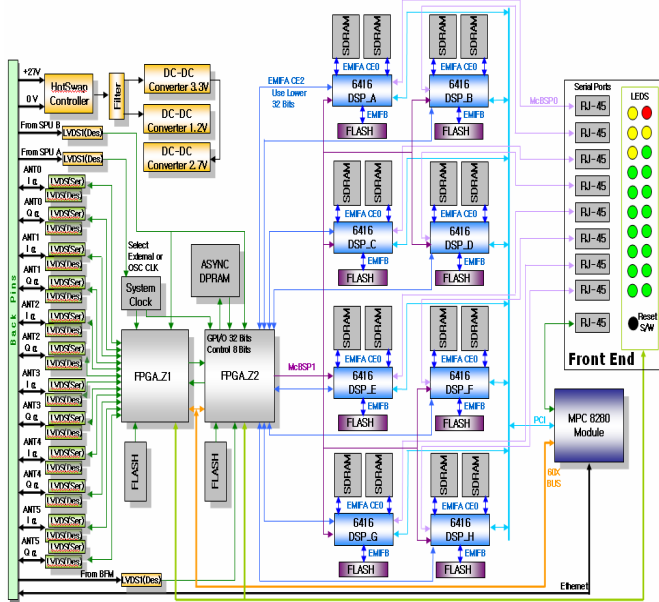


Fig. 5: Block diagram of proposed smart antenna channel card

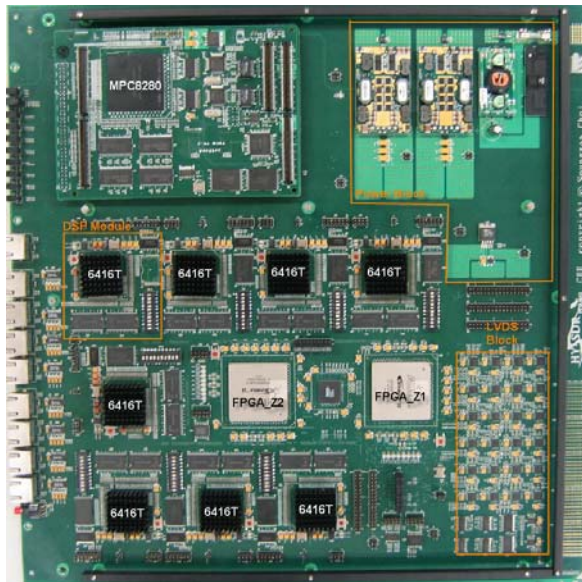


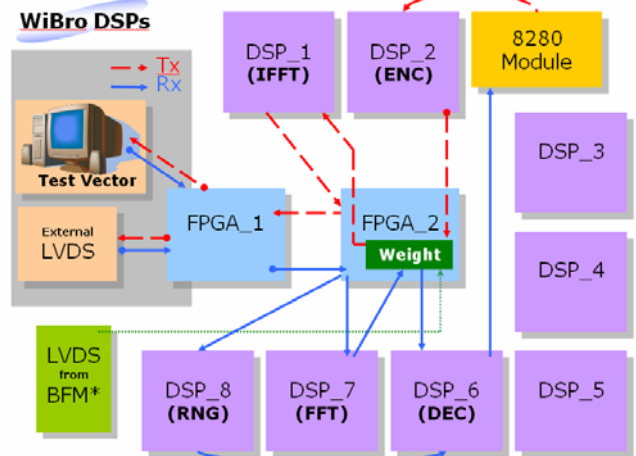
Fig. 6: Photograph of proposed smart antenna channel card

### 3.2. Functional Blocks and Signal Flows

In this Section we present the arrangements of signal flows and functional blocks for each device on the proposed smart antenna channel card supporting WiBro and TDD HSDPA.

#### 3.2.1. WiBro Implementation

Fig. 7 shows an example of allocating the functional blocks to the DSPs, FPGAs, and micro-processor. The signal flows for the WiBro mode consists of 3 divisions, described next.



\* BFM: Beam Former Card

Fig. 7: Functional blocks and signal flows for WiBro mode

First, the flow of a beamforming weight signal begins with an external beamformer card. From this the beamforming weights are transferred through the LVDS interface and stored in FPGA\_2.

Then, the flow is for a transmit signal. The data which is generated by the 8280 module that supports MAC is encoded in DSP\_2, multiplied with beamforming weights in FPGA\_2, and transferred to DSP\_1 for IFFT operation. Then the transmit signal passes through FPGA\_2 and FPGA\_1, and goes to the external card through the LVDS interface. A personal computer is connected with the channel card for performance analysis.

Finally, the flow of received signal begins with FPGA\_1. The signal is transferred to FPGA\_2 through FPGA\_1, and DSP\_8 performs an initial synchronization. At the same time FFT operation is performed in DSP\_7. After FFT the signals are weighted by beamforming weights in FPGA\_2, and then demodulated and decoded in DSP\_8. The decoded data is transferred to the 8280 module. DSPs unused in the WiBro mode could aid computational load balancing or monitoring.

#### 3.2.2. TDD HSDPA Implementation

For TDD HSDPA, Fig. 8 shows an example of functional mapping for each device. As in the WiBro mode, there are 3 main signal flows, described next.

First, the beamforming weight signal flows as in WiBro.

Then, for the flow of transmit signal DSP\_1 encodes the signals received from the 8280 module, and DSP\_2 modulates the encoded data. Modulated data is multiplied with the beamforming weights in FPGA\_2 and then converted to LVDS format in FPGA\_1 for transfer to the external card.

Finally, FPGA\_1 receives the baseband signal from the external card through LVDS interface. The baseband signals flow to FPGA\_2 for a search operation, and then to DSP\_7 for channel estimation. In addition, the signals from each antenna array element are combined with the beamforming weights, and then demodulated and detected using DSP\_6. DSP\_4 decodes the data and transfers it to the 8280 module, ending the flow for the received signals.

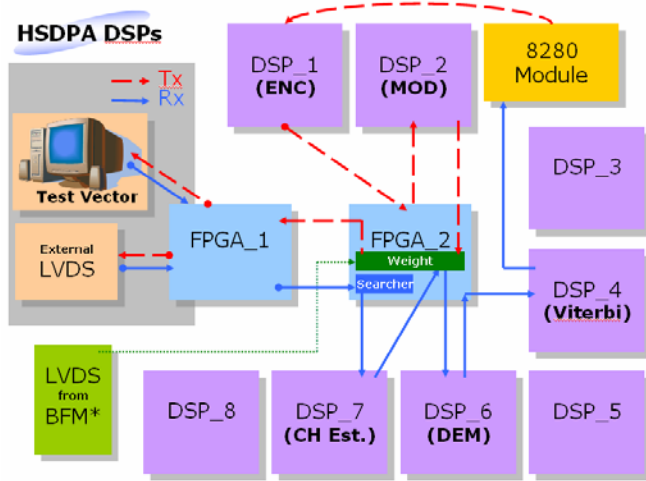


Fig. 8: Functional blocks and signal flows for TDD HSDPA mode

#### 4. PERFORMANCE EVALUATION

For a performance analysis we first download software for WiBro or TDD HSDPA mode to the channel card and generate received signals using the computer. The simulated received signal is obtained by passing random transmit signals with the format of the selected mode through a channel model. The result is then passed to the channel card, which performs the mode-specific operations defined by the downloaded software.

##### 4.1. WiBro

Fig. 9 illustrates the bit error rate (BER) obtained through computer simulations and channel card processing. In the figure legend “float\_” identifies computer simulation results. The remaining plots show results obtained using the channel card. In addition, “sas\_” stands for smart antenna with 6 antenna elements, “ideal” stands for perfect channel knowledge, and “ce\_LI” or “LI” stand for least-squares channel estimation with linear interpolation using the pilot subcarriers. Fig. 9 indicates close agreement between simulation and channel-card-based processing results. The performance degradation due to the channel estimation is about 2.5 dB vs. ideal channel knowledge. The figure also indicates a 6 dB gain with smart antenna.

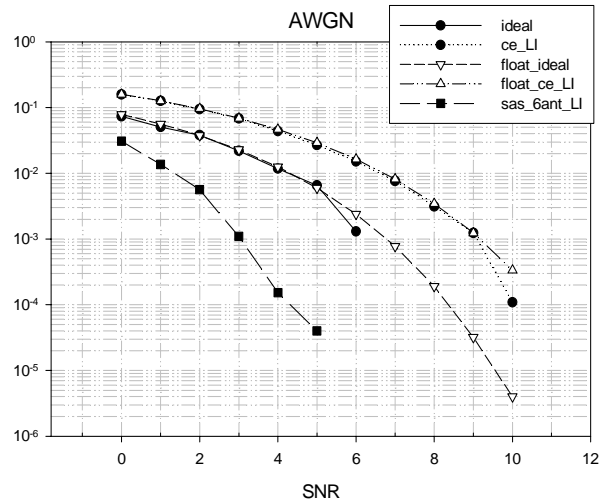


Fig. 9: Performance of WiBro in AWGN channel

##### 4.2. TDD HSDPA

Fig. 10 depicts the performance for a single antenna system with joint detection and a smart antenna system with 6 antenna elements in TDD HSDPA mode. In the figure K represents the number of users. Note that the smart antenna system yields a 6 dB gain compared to the single antenna system in AWGN channel.

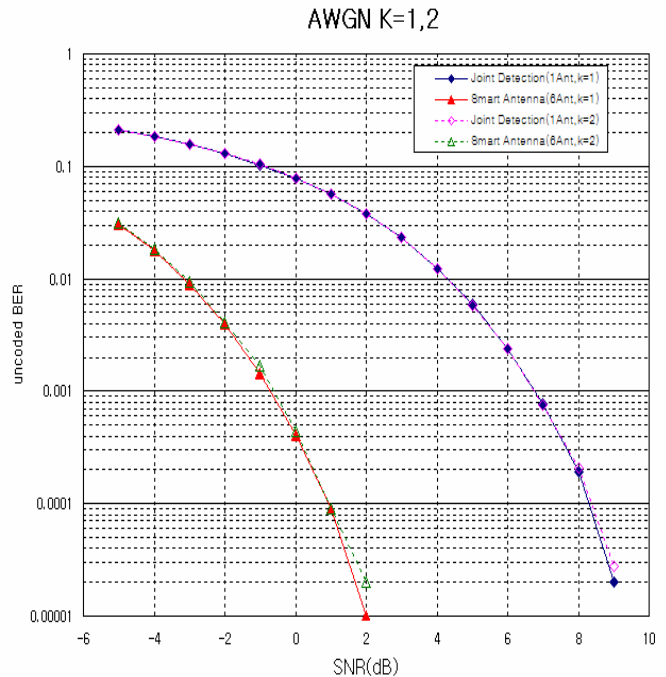


Fig. 10: Performance of TDD HSDPA in AWGN channel

## 5. CONCLUSION

This paper presents the design and performance of a new multimode channel card for SDR smart antenna base-station. We overview the transmitter and receiver block diagrams for WiBro and TDD HSDPA, and show the reference design of hardware platform for the multi-mode channel card. The proposed channel card – implemented using 8 DSPs, 2 FPGAs, and one microprocessor – supports the functional blocks required by WiBro and TDD HSDPA, including beamforming functionality. We describe an example design and the associated signal flows and functional block allocation. Finally, we analyze the performance of the proposed channel card in WiBro and TDD HSDPA mode. We determine significant performance gains from a smart antenna system.

## ACKNOWLEDGMENT

This work was supported by the HY-SDR Research Center, Hanyang University, Seoul, Korea, under the ITRC program of MIC, Korea.

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