# DEVELOPMENT OF AND INITIAL PERFORMANCE RESULTS FOR A SOFTWARE DEFINED ULTRA WIDEBAND RECEIVER

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## ABSTRACT

The vast majority of today's Ultra Wideband (UWB) communication systems are composed of application specific hardware, and do not use SDR architectures. Several major challenges are involved in developing a UWB testbed—extremely high sampling rates, huge amounts of input/output data, tremendous amount of digital processing power, and developing broadband RF hardware. These challenges are particularly daunting when Commercially available Off-The-Shelf (COTS) components are used in the development of such a system. In this paper, we describe the development of a UWB SDR Transceiver Testbed based around an 8 GHz-8 ADC Time Interleaved Sampling array and a VirtexII-Pro FPGA. One of the primary issues with the Time Interleaved Sampling array is distortion introduced into the received signal as a result of ADC mismatches. Therefore, the paper also presents initial performance results for both narrowband and ultra wideband signals and indicate that acceptable system performance can be obtained even if the ADCs are only coarsely matched.

## 1. INTRODUCTION

Impulse UWB (I-UWB) signals have been an active area of research for a number of years, as these signals provide a variety of capabilities such as: precision ranging/position location, robustness to fading/interference, and the ability to capture significant amounts of multipath energy [1]. Currently, state-of-the-art UWB communication systems are composed of application-specific hardware, and do not use Software Defined Radio (SDR) architectures. The challenges involved in developing such as communication testbed—extremely high sampling rates, huge amounts of input/output data, and a tremendous amount of digital processing power—have been fairly daunting. These challenges become particularly poignant when Commercially available Off-The-Shelf (COTS) components are used in the development of such a system.

An SDR UWB receiver, however, provides tremendous flexibility over a fixed hardware implementation. Such a receiver has the capability of supporting multiple data rates, fully customizable modulation or multiple access schemes, can adapt to the propagation environment, and can operate with custom-designed waveforms. Additionally, the use of COTS components in developing a UWB SDR provides significant time and cost savings as compared to developing a custom integrated circuit.

This paper presents an overview of the development of a Software Defined UWB Communication System Testbed based around an 8-ADC/8 GHz Time Interleaved ADC array and VirtexII-Pro FPGA. The testbed is designed to operate at a maximum data rate of 100 Mbps at a range of 10 meters, has a DC – 2.2 GHz input bandwidth, and is a fully digital implementation capable of operating with a wide variety of broadband waveforms (WLAN, Bluetooth, CDMA, etc.).

This paper is organized as follows: Section 2 discusses an overview of the receiver architecture, in particular, both the RF Front End as well as the Digital Board. Section 3 presents performance results from the individual components, as well as the system as a whole. Finally, Section 4 summarizes the results in this paper and presents conclusions.

## 2. SYSTEM OVERVIEW

A basic block diagram of the receiver is given in Figure 1, and a detailed description is contained in [2]. Essentially, the receiver consists of an analog RF front end, the ADC array and clock distribution network, a Virtex II-Pro FPGA, and a USB 2.0 interface device. The RF front end utilizes several ultra-broadband amplifiers, attenuators, and filters and feeds the received signal to the ADCs.

### 2.1 RF Front End

One of the primary design objectives for the testbed was to create an extremely flexible, general-purpose system. Therefore, the RF front end consists of only the most basic elements: a transmitter/receiver switch, low noise amplifiers and filters, and a digital step attenuator. The purpose of the RF Front End is to amplify and condition the received signal (whether a UWB pulse or other waveform) for ADC

 

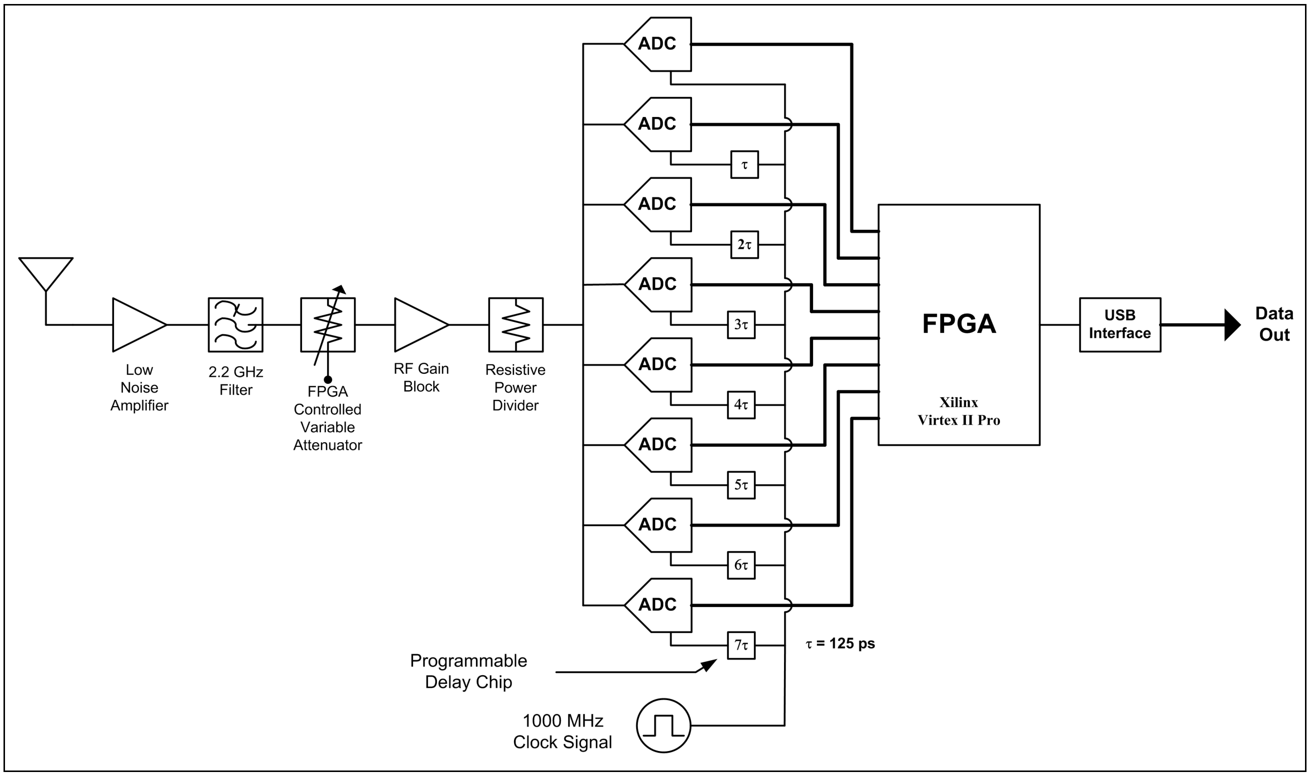


**Figure 1: Block Diagram of the UWB Receiver**

**Table 1:** Performance Summary of the RF Front End

| Parameter | Predicted Performance | Actual Performance |
|---|---|---|
| Noise Figure | 4.8 dB | 9.0 dB |
| OIP3 | 25.0 dBm | 25.4 dBm |
| Gain | 40 dB | 43 dB |
| Gain Flatness | ± 2 dB | +20 / -0 dB |
| 3 dB Bandwidth | 20 – 2700 MHz | 20 – 2200 MHz |
| Pulse Distortion | -- | 21 mV RMSE |

conversion, while imparting as little noise or distortion as possible. To save cost and time, the RF front end was implemented with discrete COTS components, although a provision was included for a custom-designed RF board to be added at a later time. Both predicted performances (as a result of both analysis and simulations) as well as measured performance results for the RF Front End are summarized in Table 1. A primary design consideration for the RF front end was to provide enough gain to allow the receiver to operate at or near the desired 10 meter range while still preserving an approximately 40 dB dynamic range and minimizing the amount of distortion introduced into the received waveform. At a range of 10 meters, both a 2 GHz CW signal as well as a UWB signal will experience approximately 60 dB of free-space path loss [1]. The transmitter produces a UWB pulse with a peak power of +20 dBm. At the receiver, the MAX 104ADCs can tolerate a maximum input signal strength of 0 dBm, and the desired SNR of the TI ADC array is 40 dB [2]. To preserve the full dynamic range, therefore, it is important to keep the noise input to the ADCs equal to or less than -40 dBm. With a predicted noise figure of 4.8 dB, and a bandwidth of 2.7 GHz, the noise power input to the RF Front End is approximately -77 dBm, resulting in a maximum tolerable gain of around 37 dB. Unfortunately, the higher measured noise figure of 9.0 dB increases the noise power input to the receiver to -72 dB, and with 43 dB of gain, results in a noise power input to the TI ADC array of -30 dBm.

To minimize signal distortion, it was desired to maintain a flat frequency response and linear phase over the entire DC-2.2 GHz operating range of the receiver. Unfortunately, the amplifiers chosen for the RF Front End were optimized for narrowband signals, and deviated significantly from the nominal frequency response, as shown in Figure 2a. This deviation introduces the small amount of pulse distortion seen in Figure 2b.

### 2.2 Digital Board

One of the primary limiting factors when implementing an UWB or Ultra Broadband SDR are the extremely high sampling frequencies required to accurately reconstruct the received waveform. As an example, for a Gaussian pulse with a time duration of 500 picoseconds (resulting in a 3 dB bandwidth of approximately 2 GHz), meeting the Nyquist criteria to recover both inphase and quadrature components

 